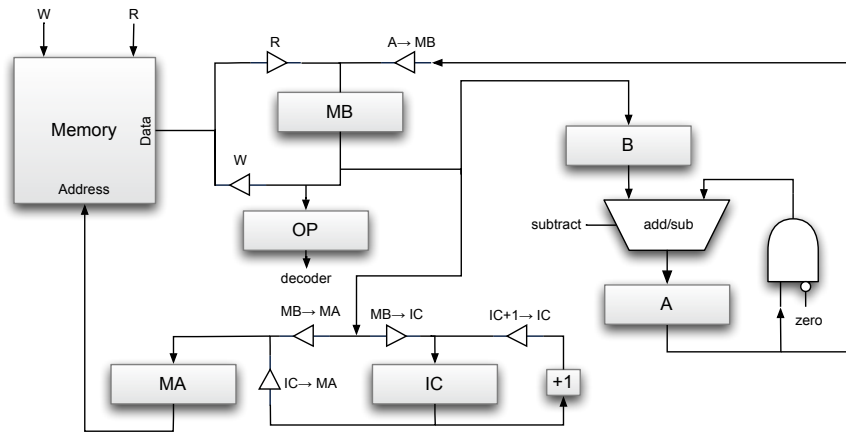
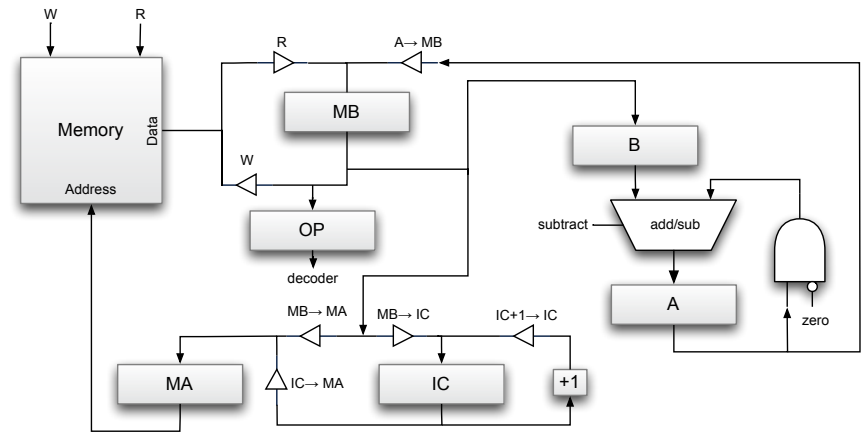


Σniac datapath

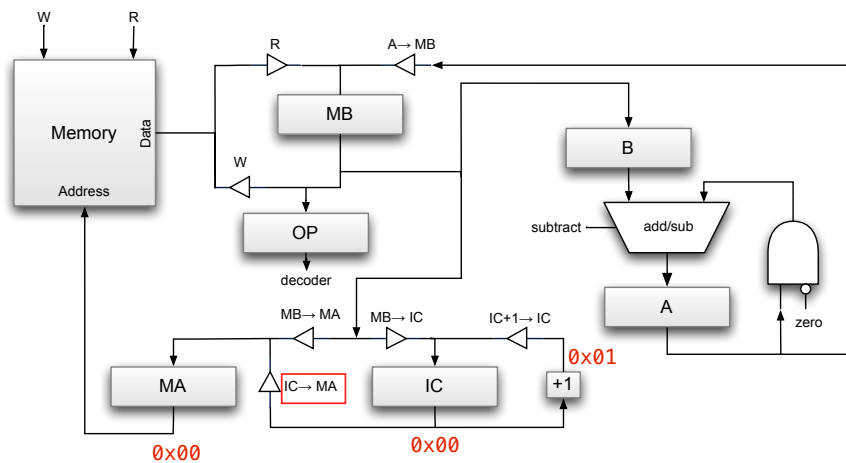


Σniac datapath



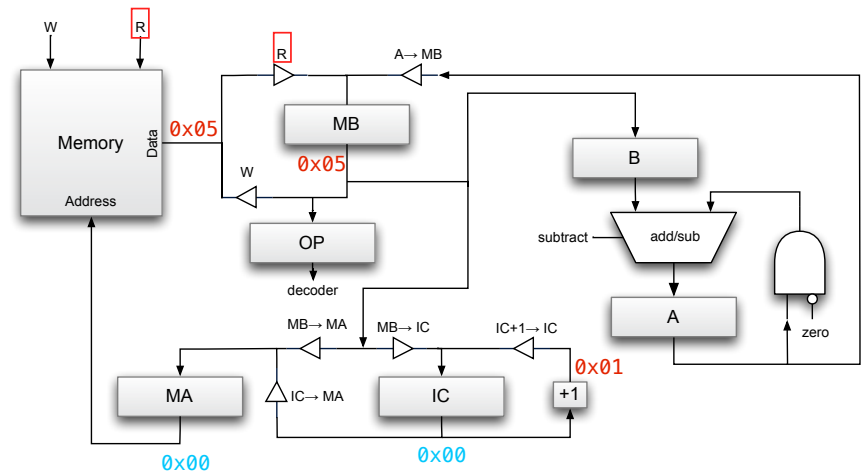
ld A, C3

Σniac datapath



ld A, C3 fetching instruction

Σniac datapath



ld A, C3 fetching instruction

Σniac datapath

Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals during instruction decoding. The components and their interactions are as follows:

- Memory:** A central component with **Address** and **Data** ports. It receives **W** (Write) and **R** (Read) signals.
- MB (Memory Buffer):** Receives **R** from Memory and outputs **W** to Memory. It also receives **A → MB** from the ALU and outputs **0x05** to the **OP** (Operation) block.
- OP (Operation):** Receives **0x05** from MB and outputs **0x0 decoder** to the **MA** (Memory Address) block.
- MA (Memory Address):** Receives **0x0 decoder** and outputs **0x00** to Memory.
- IC (Instruction Counter):** Receives **MB → IC** and outputs **0x00** to Memory. It also receives **IC → MA** from the **MA** block.
- ALU (add/sub):** Receives **B** (from Memory) and **A** (from the **A** register). It outputs **0x01** to the **A** register. It also receives **subtract** from the **zero** flag.
- A (Accumulator):** Receives **0x01** from the ALU and outputs **A → MB** to the **MB** block.
- zero:** A flag that outputs **0** to the **ALU** and **1** to the **ALU**.
- IC+1 → IC:** A control signal that increments the **IC** by 1.

The diagram shows the flow of data and control signals during instruction decoding, with specific values like **0x05**, **0x0 decoder**, **0x00**, and **0x01** indicating the state of the datapath.

Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

- Memory:** Has **Address** and **Data** ports. It receives **W** (Write) and **R** (Read) signals.
- MB (Memory Buffer):** Receives **R** (Read) from Memory and outputs **0x05** to the **OP** (Operation) block. It also receives **A → MB** from the **A** register.
- OP (Operation):** Receives **0x0** from the **decoder** and outputs **MB → MA** and **MB → IC** to the **MA** (Memory Address) and **IC** (Instruction Counter) registers, respectively.
- MA (Memory Address):** Outputs **0x05** to the **Memory** block. It receives **IC → MA** from the **IC** register.
- IC (Instruction Counter):** Outputs **0x01** to the **Memory** block. It receives **IC + 1 → IC** from the **+1** block.
- add/sub (Add/Subtract):** Receives **B** (from **MB**) and **A** (from the **A** register). It outputs **A** to the **A** register. It also receives **subtract** (from the **zero** block) and **0x01** (from the **+1** block).
- A (Accumulator):** Receives **A** from the **add/sub** block and outputs **A → MB** to the **MB** block.
- zero (Zero Flag):** Receives **A** and outputs **zero** to the **add/sub** block.
- +1 (Increment):** Receives **IC** and outputs **IC + 1 → IC** to the **IC** register.

Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

- Memory:** Has **Address** and **Data** ports. It receives **W** (Write) and **R** (Read) signals.
- MB (Memory Buffer):** Receives **R** (Read) from Memory and outputs **0x05** to the **OP** (Operation) block. It also receives **A → MB** from the **A** register.
- OP (Operation):** Receives **0x0** from the **decoder** and outputs **MB → MA** and **MB → IC** to the **MA** (Memory Address) and **IC** (Instruction Counter) registers, respectively.
- MA (Memory Address):** Outputs **0x05** to the **Memory** block. It receives **IC → MA** from the **IC** register.
- IC (Instruction Counter):** Outputs **0x01** to the **Memory** block. It receives **IC + 1 → IC** from the **+1** block.
- add/sub (Add/Subtract):** Receives **B** (from **MB**) and **A** (from the **A** register). It outputs **A** to the **A** register. It also receives **subtract** (from the **zero** block) and **0x01** (from the **+1** block).
- A (Accumulator):** Receives **A** from the **add/sub** block and outputs **A → MB** to the **MB** block.
- zero (Zero Flag):** Receives **A** and outputs **zero** to the **add/sub** block.
- +1 (Increment):** Receives **IC** and outputs **IC + 1 → IC** to the **IC** register.

Σniac datapath

Σniac datapath

[illegible]

Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

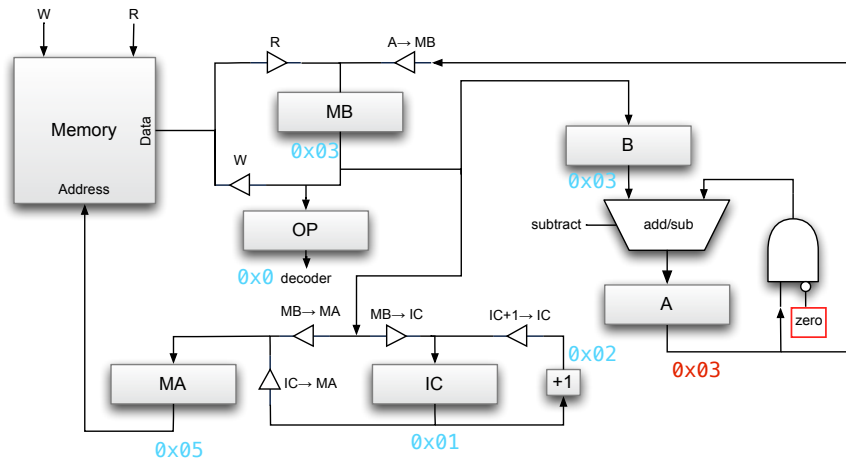
- Memory:** Has **W** (Write) and **R** (Read) ports. It outputs **Data** to the **MB** register and receives **Address** from the **MA** register.
- MB (Memory Buffer):** Receives **Data** from Memory. It has a **W** (Write) port to Memory and an **R** (Read) port to the **OP** register. It also receives **A → MB** control signals from the **A** register.
- OP (Operation):** Receives control signals from the **MB** register and outputs to the **decoder**.
- decoder:** Outputs control signals to the **MA** and **IC** registers.
- MA (Memory Address):** Receives control signals from the **decoder** and outputs **Address** to Memory. It also receives **IC → MA** control signals from the **IC** register.
- IC (Instruction Counter):** Receives control signals from the **decoder** and outputs to the **IC+1** register. It also receives **MB → IC** control signals from the **MB** register.
- IC+1:** Receives control signals from the **IC** register and outputs to the **IC** register.
- A (Accumulator):** Receives control signals from the **decoder** and outputs to the **MB** register. It also receives **IC+1 → IC** control signals from the **IC+1** register.
- B (Register):** Receives control signals from the **decoder** and outputs to the **add/sub** unit. It also receives **A → MB** control signals from the **A** register.
- add/sub (Add/Subtract):** Receives control signals from the **B** register and outputs to the **A** register. It also receives **subtract** control signals from the **decoder**.
- zero (Zero Flag):** Receives control signals from the **add/sub** unit and outputs to the **IC** register.

Control signals are labeled with hexadecimal values:

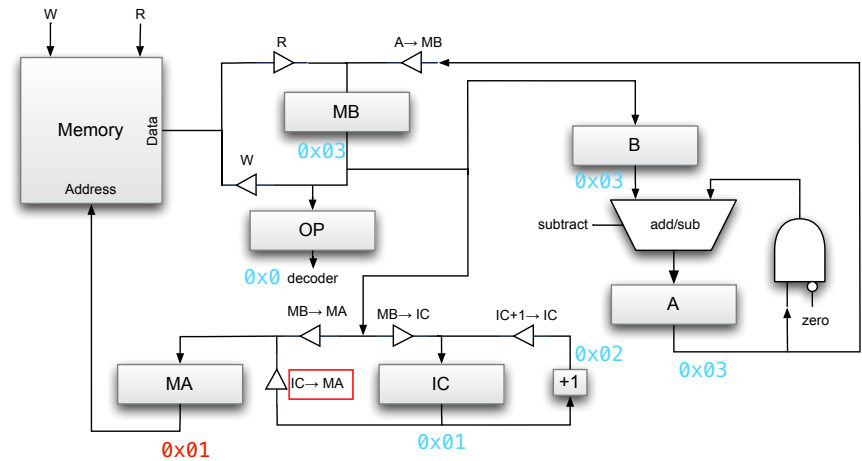
- 0x03** (red): **W** (Write) to **MB**.
- 0x00** (blue): **R** (Read) from **MB** to **OP**.
- 0x05** (blue): **Address** to **Memory**.
- 0x01** (blue): **IC → MA** control signal.
- 0x02** (blue): **IC+1 → IC** control signal.

The **add/sub** unit has a **subtract** control signal (red) and a **zero** output (blue).

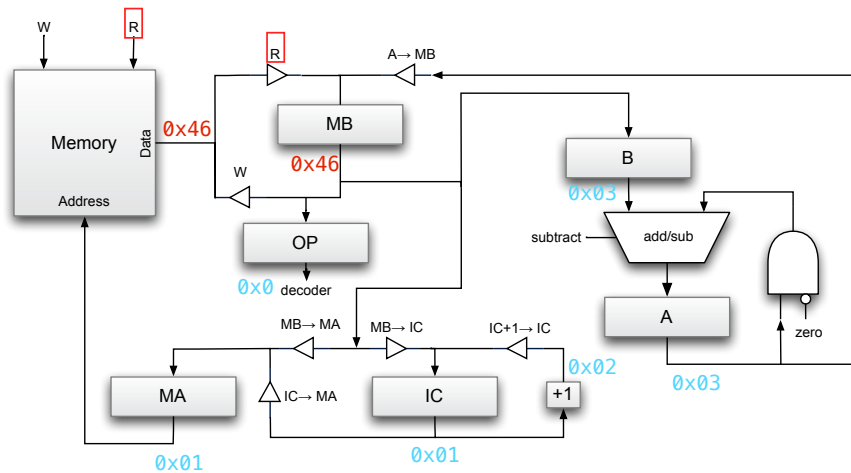
Σniac datapath



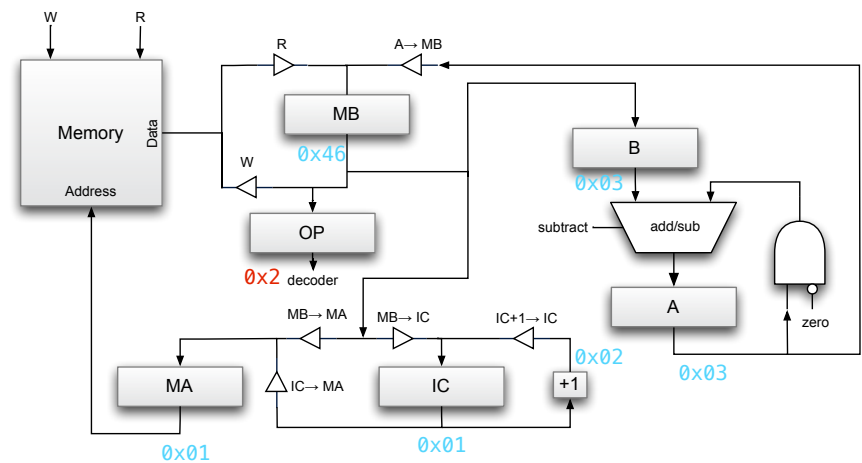
Σniac datapath



Σniac datapath



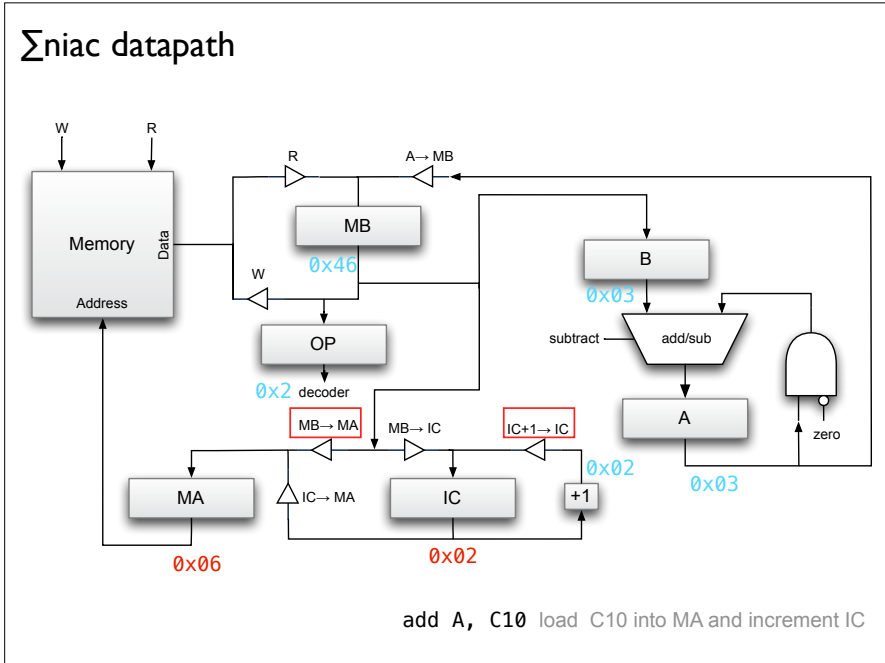
Σniac datapath



Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

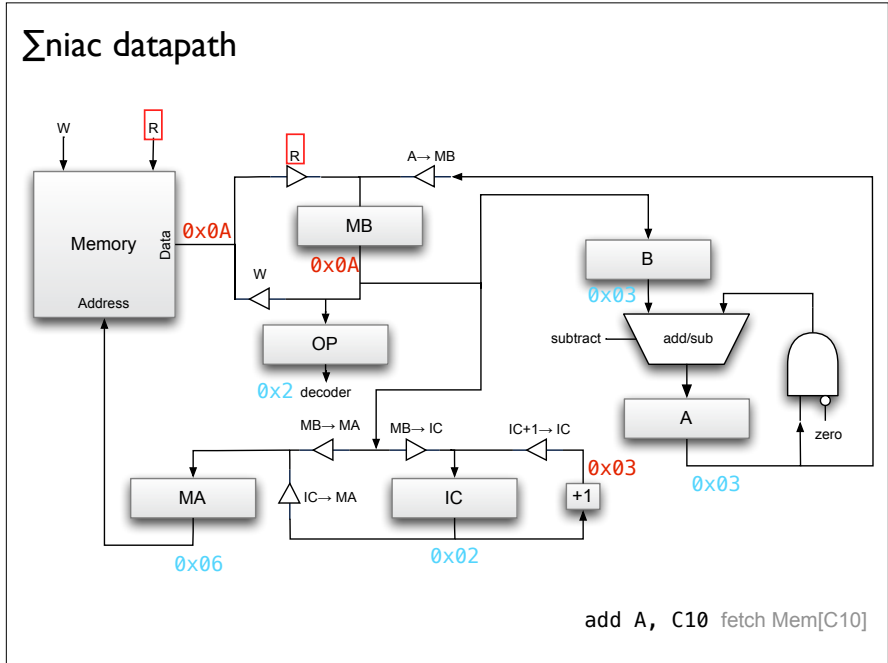
- Memory:** Has **Address** and **Data** ports. It receives **W** (Write) and **R** (Read) signals.
- MB (Memory Buffer):** Receives **R** from Memory and outputs **W** to Memory. It also receives **A → MB** and outputs **MB → MA** and **MB → IC**. A value of **0x46** is shown in blue.
- OP (Operation):** Receives **MB → MA** and outputs **0x2 decoder** to the **MA** and **IC** registers.
- MA (Memory Address Register):** Receives **MB → MA** and outputs **IC → MA** to the **IC** register. A value of **0x06** is shown in red.
- IC (Instruction Counter):** Receives **MB → IC** and **IC → MA**. It outputs **IC + 1 → IC** (highlighted in red) to a **+1** incrementer. A value of **0x02** is shown in red.
- B (Register B):** Receives **A → MB** and outputs **0x03** (in blue) to the **add/sub** unit.
- add/sub (Arithmetic/Logic Unit):** Receives **0x03** from **B** and **0x02** (in blue) from the **IC** register. It outputs to **A** and has a **subtract** control input.
- A (Register A):** Receives output from **add/sub** and outputs **A → MB** to **MB**. A value of **0x03** is shown in blue.
- zero flag:** A logic gate (AND) that outputs **zero** when both inputs are high.



Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

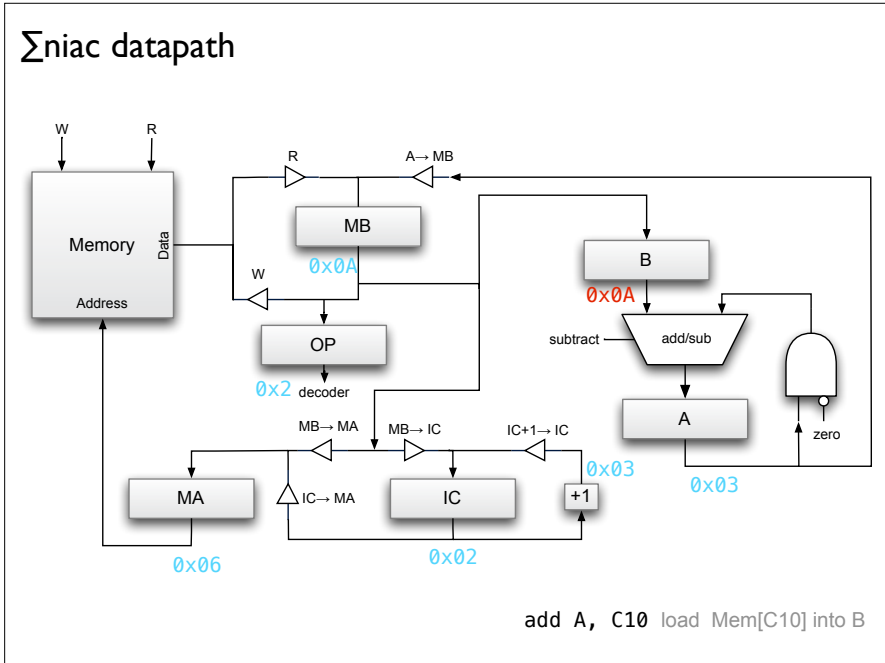
- Memory:** Receives a write address (W) and outputs data ($0x0A$) to the **MB** register and the **OP** register. It also receives a read address (R) from the **MA** register.
- MB (Memory Buffer):** Receives data from Memory and outputs it to the **OP** register and the **add/sub** unit. It also receives a read signal (R) from the **MA** register.
- OP (Operation):** Receives data from MB and outputs a control signal ($0x2$) to the **decoder**.
- decoder:** Outputs control signals ($MB \rightarrow MA$, $MB \rightarrow IC$, $IC+1 \rightarrow IC$) to the **MA**, **IC**, and **IC+1** registers.
- MA (Memory Address):** Receives control signals from the decoder and outputs a read address (R) to Memory.
- IC (Instruction Counter):** Receives control signals from the decoder and outputs a value ($0x02$) to the **IC+1** register.
- IC+1:** Receives control signals from the decoder and outputs a value ($0x03$) to the **add/sub** unit.
- add/sub (Add/Subtract):** Receives data from MB and IC+1, and outputs a result ($0x03$) to the **A** register. It also receives a control signal ($0x3$) from the **decoder**.
- A (Accumulator):** Receives data from add/sub and outputs a value ($0x03$) to the **MB** register and the **zero** flag.
- zero:** A flag that is set when the result in A is zero.



Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

- Memory:** Has **W** (Write) and **R** (Read) ports. It outputs **Data** and receives **Address**.
- MB (Memory Buffer):** Receives **0x0A** and outputs **W** to Memory and **R** to OP.
- OP (Operation):** Receives **0x2** and outputs **decoder** to MA and IC.
- MA (Memory Address):** Receives **0x06** and outputs **IC→MA** to IC.
- IC (Instruction Counter):** Receives **0x02** and outputs **MB→IC** to MB and **IC+1→IC** to the **+1** block.
- +1 (Incrementer):** Increments the IC value by 1.
- add/sub (Arithmetic Logic Unit):** Receives **0x0A** and **0x03**. It has a **subtract** control signal and outputs to **A**.
- A (Accumulator):** Receives the output from the add/sub block and outputs **0x03** to the **zero** block.
- zero (Zero Flag):** A logic block that outputs **0x03** to the add/sub block.
- Control Signals:**
 - 0x0A:** A red signal that branches to MB, the add/sub block, and the zero flag.
 - 0x2:** A blue signal that branches to the OP block and the MA block.
 - 0x06:** A blue signal that branches to the MA block and the IC block.
 - 0x03:** A blue signal that branches to the add/sub block and the zero flag.
 - 0x02:** A blue signal that branches to the IC block and the MA block.



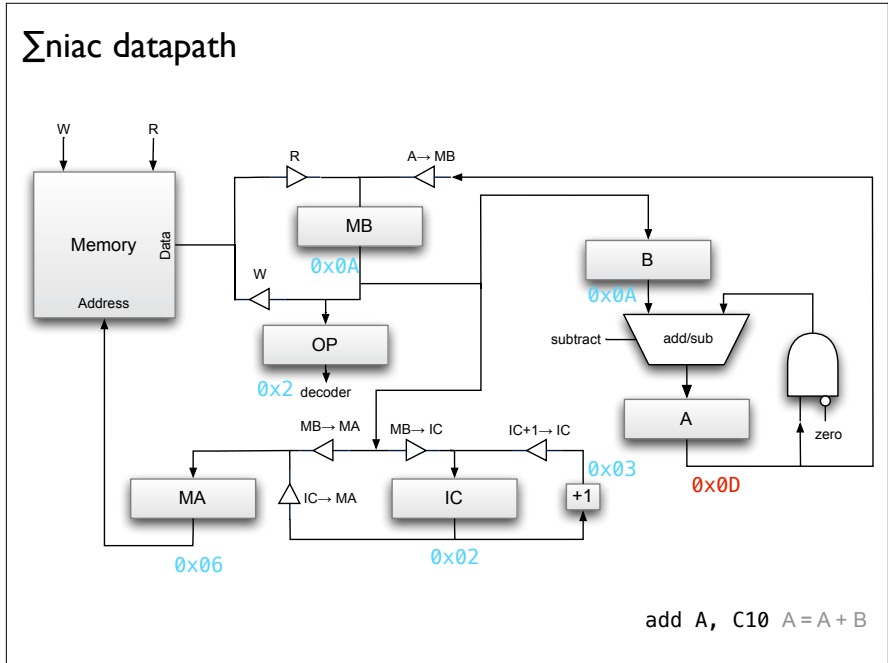
Σniac datapath

The diagram illustrates the Σniac datapath, showing the flow of data and control signals between various components:

- Memory:** Receives **Address** and outputs **Data**. It has **W** (Write) and **R** (Read) control inputs.
- MB (Memory Buffer):** Receives **W** and **R** control signals. It outputs **0x0A** to the **OP** (Operation) block and **0x0A** to the **add/sub** block.
- OP (Operation):** Receives **0x0A** from the **MB** and outputs **0x2** to the **decoder**.
- decoder:** Outputs **MB → MA** and **MB → IC** control signals.
- MA (Memory Address):** Receives **MB → MA** and outputs **0x06** to the **Memory** block.
- IC (Instruction Counter):** Receives **MB → IC** and outputs **0x02** to the **Memory** block.
- IC+1 → IC:** Receives **0x02** and outputs **0x03** to the **IC** block.
- add/sub (Add/Subtract):** Receives **0x0A** from the **MB** and **0x0D** from the **zero** block. It outputs **0x0D** to the **A** (Accumulator) block.
- A (Accumulator):** Receives **0x0D** from the **add/sub** block and outputs **0x0D** to the **zero** block.
- zero:** Receives **0x0D** from the **A** block and outputs **0x0D** to the **add/sub** block.
- Control Signals:**
 - W (Write):** Controls the **Memory** and **MB** blocks.
 - R (Read):** Controls the **Memory** and **MB** blocks.
 - A → MB:** Controls the **MB** block.
 - MB → MA:** Controls the **MA** block.
 - MB → IC:** Controls the **IC** block.
 - IC+1 → IC:** Controls the **IC** block.
 - IC → MA:** Controls the **MA** block.

The diagram also includes a legend for the control signals:

- 0x0A:** Blue text, associated with the **MB** block.
- 0x02:** Blue text, associated with the **IC** block.
- 0x03:** Blue text, associated with the **IC+1 → IC** block.
- 0x06:** Blue text, associated with the **MA** block.
- 0x0D:** Red text, associated with the **A** (Accumulator) block.



I

	000 ld	001 sub	010 add	011 st	100 b	101 bneg	111 halt
t0	Mem $\Rightarrow$ MB: R, ld_mb						
t1	MB $\Rightarrow$ OP: ld_op						
t2	Inc IC: IC+1>IC, ld_ic				MB>IC, ld_ic	A?>0:IC + 1>IC A?>1:PB>IC IC<5	halt
t3	MB>MA, ld_ma, set E				IC>MA, ld_ma		

E

t0	Mem $\Rightarrow$ MB: R, ld_mb			A>MB, ld_mb
t1	MB $\Rightarrow$ B: ld_b			MB $\Rightarrow$ Mem: w
t2	zero, ld_a	sub, ld_a	ld_a	-
t3	IC>MA, ld_ma, reset E			